Findlater teaches how pins between the MAC and PHY may be used to multiplex data. In particular, as discussed in column 8, lines 14-18 of Findlater, the RXD1 time slot is used to indicate a data rate, where RXD1 = 1 indicates 100 Mbit/s and RXD1=0 indicates 10 Mbit/s.

Nowhere does Findlater teach or suggest a word based interface between a MAC and a PHY. A word comprises fields, where a field is one or more specific positions in the word and is interpreted according to some protocol. Using a word based interface provides a great deal of flexibility. In particular, in the present invention, the speed by which the MAC and PHY communicate data to each other is adaptive. Whereas Findlater teaches how a time slot may be used to provide up to two data speeds, the present invention utilizes a word based interface, so that the data speed between the PHY and MAC is adaptive. That is, the speeds of the present invention are not limited to some fixed set of speeds, such as 10 Mbit/s or 100 Mbit/s.

As discussed in the specification of the present application, page 5, lines 4-20, various types of word formats are supported, depending upon the Rx_Dv field. If this field is zero, then the PHY-to-MAC words provide control information. In particular, bit position number 9 (see Fig. 2 of the present application) of a control word is the Tx_Cyc field. If Tx_Cyc = 1, then the PHY is ready for data from the MAC. If Tx_Cyc is zero, then the PHY is not ready for data from the MAC. Specifically, as claimed in claim 1, the "slow mode PHY-to-MAC words include a transmit cycle field to indicate whether the MAC is to provide data in a next MAC-to-PHY word." In this way, many data speeds may be supported in a flexible manner without changing the clock signal frequency, because the MAC may or may not provide data in the next MAC-to-PHY word, depending upon whether the transmit cycle field in the PHY-to-MAC word is a 1 or 0.

Nowhere does Findlater teach or suggest the claimed limitation of a slow mode PHY-to-MAC word that includes a transmit cycle filed to indicate whether the MAC is to provide data in the next MAC-to-PHY word. Consequently, Applicant believes that claim 1, and claim 2 by virtue of its dependency upon claim 1, are patentable over Findlater.

Claim 8 also includes the limitation "wherein the slow mode PHY-to-MAC words include a transmit cycle field to indicate whether the MAC is requested by the PHY to provide data for transmission on the medium in a next MAC-to-PHY word."

Consequently, claim 8, and claim 9 by virtue of its dependency upon claim 8, are believed patentable over Findlater.

The last "wherein" clause of claim 15 also recites the transmit cycle field in a slow mode PHY-to-MAC word, where if the transmit cycle field is a first value, then the MAC is requested to transmit data in a second MAC-to-PHY word, and if the transmit cycle field is a second value, then the MAC is not requested to provide transmit data. Again, for the same reasons as stated above with respect to claim 1, Findlater neither teaches nor suggests this claim limitation. Consequently, claim 15, and claim 16 by virtue of its dependency upon claim 15, are believed patentable over Findlater.

Regarding the rejection of claims 3-7, 10-14, and 17-21, Rubin is cited merely for teaching words that are each 12 bits wide, as well as teaching an equal speed mode word. As discussed above, Findlater neither teaches nor suggests the claim limitations regarding the transmit cycle field and how this field controls whether or not the MAC is requested to provide data in the next MAC-to-PHY word. Because all the independent claims have this type of claim limitation, as discussed earlier, all claims are believed patentable over Rubin and Findlater.

Respectfully submitted,

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